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10/713,486	11/14/2003	Howard S. David	0294374 p15159	9195

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EXAMINER	
DARE, RYAN A	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,486	DAVID, HOWARD S.	
	Examiner	Art Unit	
	RYAN DARE	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-9,12-17,19,21-23,25-31,33-38 and 40-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-9,12-17,19,21-23,25-31,33-38 and 40-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/24/09,2/26/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 5, 12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, US PG Pub 2004/0093461, in view Tsern et al., US Patent 6,343,042.

3. With respect to claim 5, Kim teaches a method of operating a memory device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals, in pars. 23-24;

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, in pars. 23-24 and 27-28.

Kim fails to teach a staggered refresh. Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

4. It would be obvious to one of ordinary skill in the art, having the teachings of Kim and Tsern before him at the time the invention was made, to modify the memory refresh

method of Kim with the memory refresh system of Tsern, in order to control refreshing noise by avoiding current spikes, as taught by Tsern in col. 2, lines 30-38.

5. With respect to claim 12, Applicant claims an article comprising a storage medium having stored thereon instructions that when executed by a machine result in performing the method of claim 5, and is therefore rejected using similar logic.

6. With respect to claim 21, Kim teaches a memory device responsive to command signals and bank address signals, the memory device comprising:

multiple memory bank arrays, each memory bank array having storage cells, in the Abstract; and

a command controller/decoder responsive to selected command signals and bank address signals to initiate an auto-refresh command controlling an auto refresh operation to at least one specified memory bank array of the multiple memory bank arrays, in fig. 3, command decoder 20, and par. 36.

Kim fails to teach a staggered refresh. Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the auto-refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

7. It would be obvious to one of ordinary skill in the art, having the teachings of Kim and Tsern before him at the time the invention was made, to modify the memory refresh method of Kim with the memory refresh system of Tsern, in order to Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are

refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

8. Claims 1-2, 6-9, 13-15, 23, 25-31, 33-38 and 40-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, US PG Pub 2004/0093461, in view of Proebsting, US Patent 6,871,261, further in view of Tsern.

9. With respect to claim 1, Kim teaches a method of operating a memory device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals, in pars. 23-24;

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, in pars. 23-24 and 27-28.

Kim fails to teach the last limitation of claim 1. Proebsting teaches initiating, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, the second operation begins after all the rows have begun the auto refresh operation, in col. 2, lines 43-50.

Kim and Proebsting fail to teach a staggered refresh. Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

10. It would be obvious to one of ordinary skill in the art, having the teachings of Kim and Proebsting before him at the time the invention was made, to modify the memory refresh method of Kim with the memory refresh method of Proebsting, because it allows both operations to complete in the same clock cycle as taught by Proebsting in col. 2, lines 43-47. This makes it so that a read or write does not have to be stalled as long as the particular memory bank array is not being accessed, and thus saves time. Furthermore, it would be obvious to one of ordinary skill in the art, having the teachings of Kim, Proebsting and Tsern before him at the time the invention was made, to modify the memory refresh method of Kim and Proebsting with the memory refresh system of Tsern, in order to Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

11. With respect to claim 2, Kim teaches the method of claim 1, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received, in pars. 27-28.

12. With respect to claim 6, Kim, Proebsting and Tsern teach all other limitations of the parent claim as discussed supra, but implements the invention on a DRAM and not on an SDRAM. As is known in the art, a SDRAM is simply a DRAM that employs a bursting technique that predicts the next memory location to be accessed. Therefore, benefits achieved by Kim's invention will have the same positive effect on an SDRAM as it will on a non-synchronous DRAM.

13. It would have been obvious to one of ordinary skill in the art at the time the invention was made, to implement the present invention on an SDRAM since this is a type of a DRAM which will also use the benefits achieved by the Kim invention, such as reducing power consumption and decreasing noise by reducing peak operation current, as taught by Kim in the last sentence of the Abstract.

14. With respect to claim 13, Applicant claims an article comprising a storage medium having stored thereon instructions that when executed by a machine result in performing the method of claim 6, and is therefore rejected using similar logic

15. With respect to claim 7, the combination of Kim, Proebsting and Tsern teaches all other limitations of the parent claim as discussed supra. Proebsting further teaches the method of claim 3, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations, in col. 2, lines 43-50. Although Proebsting only mentions read and write operations, in view of Applicant's Related Art, it is inherent that these include activate and precharge operations. Applicant discloses that access operations include activate and precharge operations in page 1, line 17, through page 2, line 13. Therefore,

Proebsting also teaches performing activate and precharge operations since these are inherent to the read and write operations it discloses.

16. With respect to claims 8-9, Applicant claims an article comprising a storage medium having stored thereon instructions that when executed by a machine result in performing the method of claims 1-2, and are therefore rejected using similar logic.

17. With respect to claim 14, Applicant claims an article comprising a storage medium having stored thereon instructions that when executed by a machine result in performing the method of claim 7, and is therefore rejected using similar logic.

18. With respect to claim 15, Kim teaches a memory device responsive to command signals and bank address signals, the memory device comprising:

multiple memory bank arrays, each memory bank array having storage cells, in the Abstract; and

a command controller/decoder responsive to selected command signals and bank address signals to initiate an auto-refresh command controlling an auto refresh operation to at least one specified memory bank array of the multiple memory bank arrays, in fig. 3, command decoder 20, and par. 36.

Kim fails to teach the last part of claim 1. Proebsting teaches: before or during the auto refresh operation to the at least one of the specified memory bank arrays, issuing a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, in col. 2, lines 43-50.

Kim and Proebsting fail to teach a staggered refresh. Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

It would be obvious to one of ordinary skill in the art, having the teachings of Kim and Proebsting before him at the time the invention was made, to modify the memory refresh method of Kim with the memory refresh method of Proebsting, because it allows both operations to complete in the same clock cycle as taught by Proebsting in col. 2, lines 43-47. This makes it so that a read or write does not have to be stalled as long as the particular memory bank array is not being accessed, and thus saves time. Furthermore, it would be obvious to one of ordinary skill in the art, having the teachings of Kim, Proebsting and Tsern before him at the time the invention was made, to modify the memory refresh method of Kim and Proebsting with the memory refresh system of Tsern, in order to Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

19. With respect to claim 23, Proebsting teaches the memory device of claim 15, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations, in col. 2, lines

43-50. Although Proebsting only mentions read and write operations, in view of Applicant's Related Art, it is inherent that these include activate and precharge operations. Applicant discloses that access operations include activate and precharge operations in page 1, line 17, through page 2, line 13. Therefore, Proebsting also teaches performing activate and precharge operations since these are inherent to the read and write operations it discloses.

20. With respect to claim 26, Kim teaches a method of operating a device having multiple memory bank arrays and being responsive to command signals and a plurality of bank address signals, the method comprising:

specifying at least one of a multiple of memory bank arrays to be refreshed using a plurality of bank address signals, in pars. 23-24; and

initiating in response to first command signals an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays, wherein multiple rows per memory bank array are refreshed per auto-refresh command, in pars. 23-24 and 27-28.

Proebsting teaches:

initiating, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command signal controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, in col. 2, lines 43-50.

Kim and Proebsting fail to teach a staggered refresh. Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

21. It would be obvious to one of ordinary skill in the art, having the teachings of Kim and Proebsting before him at the time the invention was made, to modify the memory refresh method of Kim with the memory refresh method of Proebsting, because it allows both operations to complete in the same clock cycle as taught by Proebsting in col. 2, lines 43-47. This makes it so that a read or write does not have to be stalled as long as the particular memory bank array is not being accessed, and thus saves time. Furthermore, it would be obvious to one of ordinary skill in the art, having the teachings of Kim, Proebsting and Tsern before him at the time the invention was made, to modify the memory refresh method of Kim and Proebsting with the memory refresh system of Tsern, in order to Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

22. With respect to claim 25, Kim teaches a method of claim 26, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received, in pars. 27-28.

23. With respect to claim 27, Kim, Proebsting and Tsern teach all other limitations of the parent claim as discussed supra, but implements the invention on a DRAM and not on an SDRAM. As is known in the art, a SDRAM is simply a DRAM that employs a bursting technique that predicts the next memory location to be accessed. Therefore, benefits achieved by Kim, Proebsting's and Tsern's invention will have the same positive effect on an SDRAM as it will on a non-synchronous DRAM.

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made, to implement the invention of Kim, Proebsting and Tsern on an SDRAM since this is a type of a DRAM which will also use the benefits achieved by the Kim, Proebsting and Tsern inventions, such as reducing power consumption and decreasing noise by reducing peak operation current, as taught by Kim in the last sentence of the Abstract.

25. With respect to claim 28, Kim, Proebsting and Tsern teach all other limitations of the parent claim as discussed supra. Proebsting further teaches the method of claim 26, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations, in col. 2, lines 43-50. Although Proebsting only mentions read and write operations, in view of Applicant's Related Art, it is inherent that these include activate and precharge operations. Applicant discloses that access operations include activate and precharge operations in page 1, line 17, through page 2, line 13. Therefore, Proebsting also teaches performing activate and precharge operations since these are inherent to the read and write operations it discloses.

26. With respect to claim 29, Kim, Proebsting and Tsern teach all other limitations of the parent claims as discussed supra. Proebsting further teaches the method of claim 28, wherein second command signals, to initiate an activate operation to open a page not to be refreshed, are issued by the memory controller after first command signals to initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays to be refreshed, in preparation for issuing second command signals to initiate read operations or write operations to the open page. Although Proebsting does not expressly mention performing the activate operation before the read or write, it would be obvious to one of ordinary skill in the art to do activate a row before reading from it. This is taught by Applicant in the Discussion of Related Art on page 2, lines 3-13. Since an activation is a necessary part of a read or write, this would be an essential and obvious operation to perform.

27. With respect to claim 30, Kim teaches a memory controller for controlling a memory device having multiple memory bank arrays comprising:

a processor for scheduling and generating a plurality of bank address signals, first command signals, and second command signals, wherein the plurality of bank address signals specifies at least one of a multiple of memory bank arrays to be refreshed, the first command signals initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of multiple memory bank arrays, in pars. 23-24 and 27-28. Kim fails to teach the second command signals that read or write from another memory bank array.

Proebsting teaches second command signals that initiate, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, in col. 2, lines 43-50.

Kim and Proebsting fail to teach a staggered refresh. Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

28. It would be obvious to one of ordinary skill in the art, having the teachings of Kim and Proebsting before him at the time the invention was made, to modify the memory refresh method of Kim with the memory refresh method of Proebsting, because it allows both operations to complete in the same clock cycle as taught by Proebsting in col. 2, lines 43-47. This makes it so that a read or write does not have to be stalled as long as the particular memory bank array is not being accessed, and thus saves time. Furthermore, it would be obvious to one of ordinary skill in the art, having the teachings of Kim, Proebsting and Tsern before him at the time the invention was made, to modify the memory refresh method of Kim and Proebsting with the memory refresh system of Tsern, in order to Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other

rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

29. With respect to claim 31, Kim teaches the memory controller of claim 30, wherein the specified at least one of the multiple memory bank arrays is specified in logic based on the plurality of bank address signals received, in pars. 27-28.

30. With respect to claim 33, Kim teaches a memory controller for controlling a memory device having multiple memory bank arrays comprising:

a processor for scheduling and generating a plurality of bank address signals, first command signals, and second command signals, wherein the plurality of bank address signals specifies at least one of a multiple of memory bank arrays to be refreshed, the first command signals initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of multiple memory bank arrays, in pars. 23-24 and 27-28. Kim fails to teach the second command signals that read or write from another memory bank array.

Proebsting teaches second command signals that initiate, before or during the auto refresh operation to the at least one of the specified memory bank arrays, a second command controlling a second operation, other than an auto refresh operation, to a second memory bank array of the multiple memory bank arrays, which is not one of the at least one of the specified memory bank arrays being refreshed, in col. 2, lines 43-50.

Kim and Proebsting fail to teach a staggered refresh. T Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

31. It would be obvious to one of ordinary skill in the art, having the teachings of Kim and Proebsting before him at the time the invention was made, to modify the memory refresh method of Kim with the memory refresh method of Proebsting, because it allows both operations to complete in the same clock cycle as taught by Proebsting in col. 2, lines 43-47. This makes it so that a read or write does not have to be stalled as long as the particular memory bank array is not being accessed, and thus saves time. Furthermore, it would be obvious to one of ordinary skill in the art, having the teachings of Kim, Proebsting and Tsern before him at the time the invention was made, to modify the memory refresh method of Kim and Proebsting with the memory refresh system of Tsern, in order to Tsern teaches a staggered refresh wherein multiple rows of the at least one memory bank array are refreshed in a staggered fashion relative to the other rows in the memory bank array per the refresh, in col. 6, lines 1-12, where one row in each bank is refreshed at a time, before moving on to the next row, thus the rows being refreshed in a staggered fashion.

32. With respect to claim 34, Kim and Proebsting teach all other limitations of the parent claim as discussed supra, but implement the invention on a DRAM and not on an SDRAM. As is known in the art, a SDRAM is simply a DRAM that employs a bursting

technique that predicts the next memory location to be accessed. Therefore, benefits achieved by Kim and Proebsting's invention will have the same positive effect on an SDRAM as it will on a non-synchronous DRAM.

33. It would have been obvious to one of ordinary skill in the art at the time the invention was made, to implement the invention of Kim and Proebsting on an SDRAM since this is a type of a DRAM which will also use the benefits achieved by the Kim and Proebsting inventions, such as reducing power consumption and decreasing noise by reducing peak operation current, as taught by Kim in the last sentence of the Abstract.

34. With respect to claim 35, the combination of Kim and Proebsting teaches all other limitations of the parent claim as discussed supra. Proebsting further teaches the memory controller of claim 30, wherein the second operation is selected from the group consisting of activate operations, read operations, write operations and precharge operations, in col. 2, lines 43-50. Although Proebsting only mentions read and write operations, in view of Applicant's Related Art, it is inherent that these include activate and precharge operations. Applicant discloses that access operations include activate and precharge operations in page 1, line 17, through page 2, line 13. Therefore, Proebsting also teaches performing activate and precharge operations since these are inherent to the read and write operations it discloses.

35. With respect to claim 36, Kim and Proebsting teach all other limitations of the parent claims as discussed supra. Proebsting further teaches the memory controller of claim 35, wherein second command signals, to initiate an activate operation to open a page not to be refreshed, are issued by the memory controller after first command

signals to initiate an auto-refresh command controlling an auto refresh operation to the specified at least one of the multiple memory bank arrays to be refreshed, in preparation for issuing second command signals to initiate read operations or write operations to the open page. Although Proebsting does not expressly mention performing the activate operation before the read or write, it would be obvious to one of ordinary skill in the art to do activate a row before reading from it. This is taught by Applicant in the Discussion of Related Art on page 2, lines 3-13. Since an activation is a necessary part of a read or write, this would be an essential and obvious operation to perform.

36. With respect to claims 37-38 and 40-43, Applicant claims a system that comprises the memory device and controller of claims 30-31 and 33-36, and is therefore rejected using similar logic.

37. Claims 16-17, 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, Proebsting and Tsern as applied to claims 1-2, 6-9, 13-15, 23, 25-31, 33-38 and 40-43 above, in view of Zheng, US Patent 6,195,303.

38. With respect to claim 16, Kim, Proebsting and Tsern teach all other limitations of the parent claim as discussed supra, but fails to teach an order of refreshing as described in claim 16. Zheng teaches a memory device, wherein the at least one specified memory bank array of the multiple memory bank arrays is determined based on which memory bank arrays have been refreshed and a subsequent known order of refreshing the memory bank arrays, in col. 3, lines 33-39.

39. It would have been obvious to one of ordinary skill in the art, having the teachings of Kim, Proebsting, Tsern, and Zheng before him at the time the invention was made, to modify the memory refresh method of Kim, Proebsting and Tsern with the memory refresh method of Zheng, in order to reduce the overhead required to operate the DRAM, since refreshes will occur automatically without external commands, and will be timed such that data is never lost, as taught by Zheng in col. 12, lines 1-9.

40. With respect to claim 17, Zheng teaches the method of claim 16, wherein the at least one specified memory bank array of the multiple memory bank arrays is determined based on a command specifying which bank is to be next refreshed and a subsequent known order of refreshing the memory bank arrays, in col. 3, lines 33-39.

41. With respect to claim 19, Zheng teaches the memory device of claim 15, further comprising a refresh counter for incrementing an address of a row to be refreshed, wherein the refresh counter has a separate counter portion for each of the multiple memory bank arrays, in col. 9, lines 12-20.

42. With respect to claim 22, Kim, Proebsting, Tsern and Zheng teach all other limitations of the parent claim as discussed supra, but implements the invention on a DRAM and not on an SDRAM. As is known in the art, a SDRAM is simply a DRAM that employs a bursting technique that predicts the next memory location to be accessed. Therefore, benefits achieved by Kim and Zheng's invention will have the same positive effect on an SDRAM as it will on a non-synchronous DRAM.

43. It would have been obvious to one of ordinary skill in the art at the time the invention was made, to implement the invention of Kim and Zheng on an SDRAM since

this is a type of a DRAM which will also use the benefits achieved by the Kim and Zheng inventions, such as reducing power consumption and decreasing noise by reducing peak operation current, as taught by Kim in the last sentence of the Abstract.

Response to Arguments

44. Applicant's arguments with respect to claims 1, 2, 5-9,12-17,19, 21-23,25-31,33-38, and 40-43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN DARE whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ryan Dare/
August 3, 2008

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186